

FIG. 1

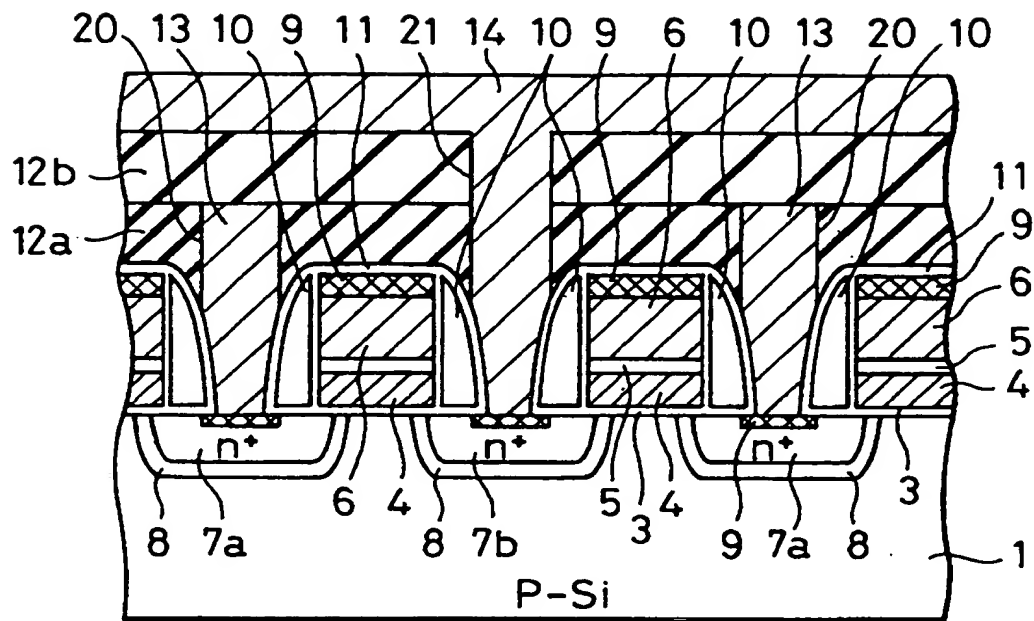


FIG. 2 (a)

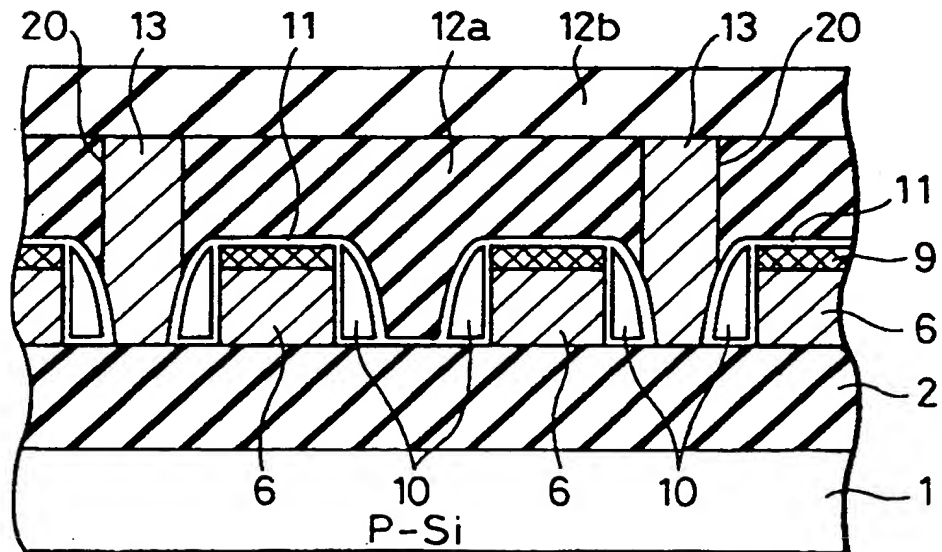


FIG. 2 (b)

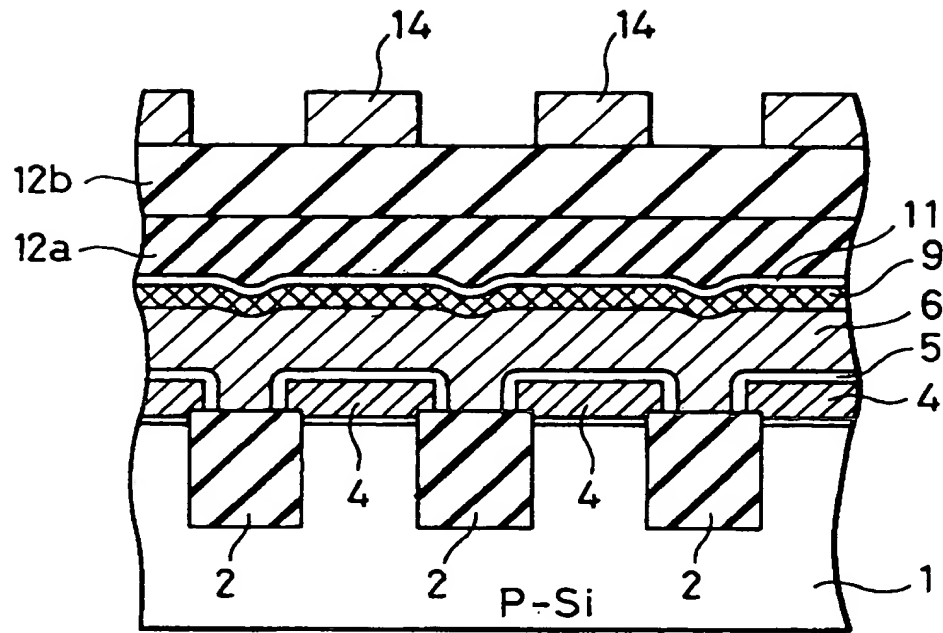


FIG. 3 (a)

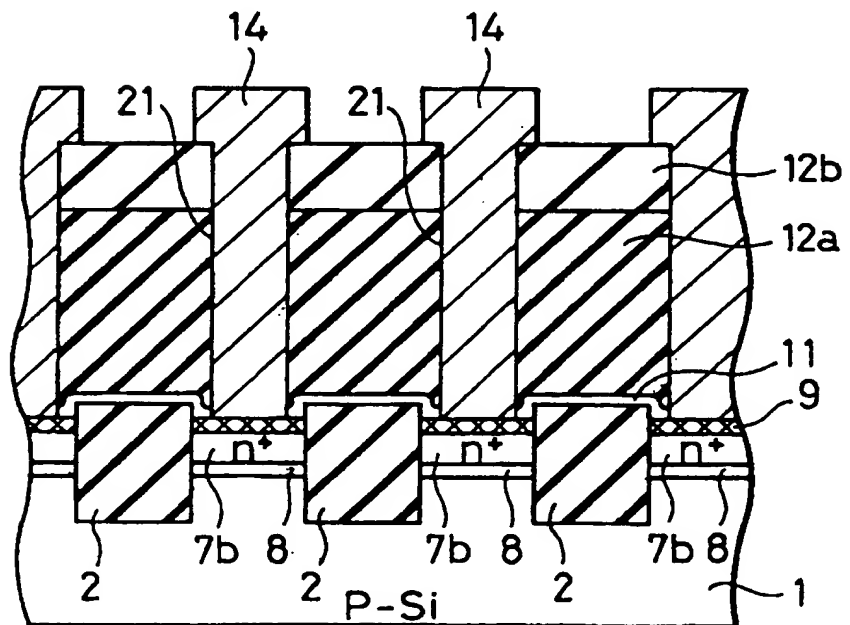
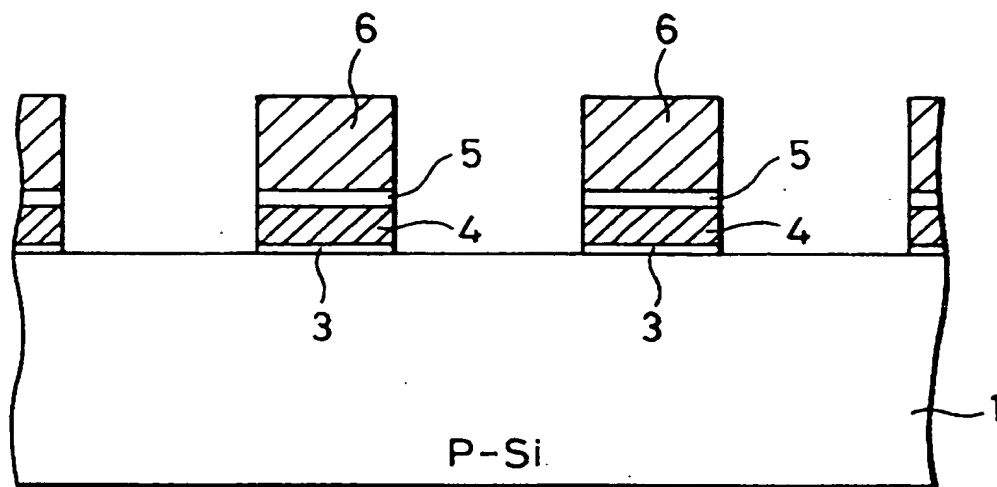
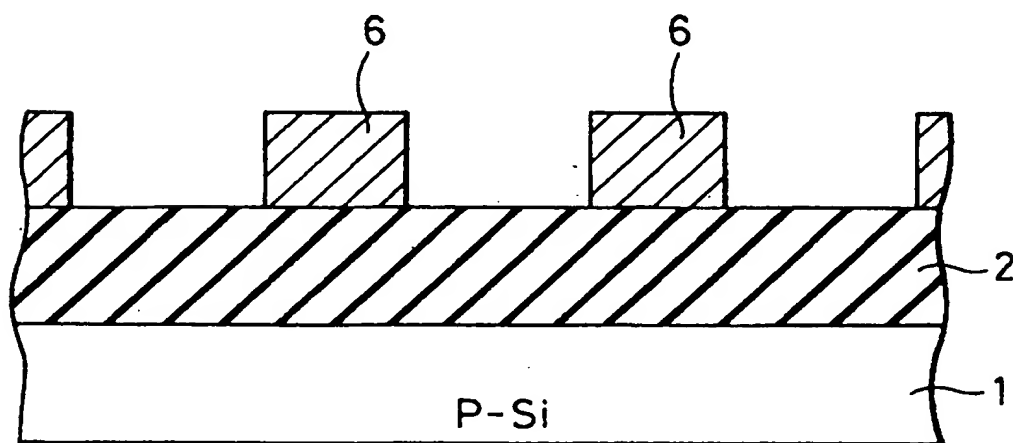


FIG. 3 (b)



F I G. 4 (a)



F I G. 4 (b)

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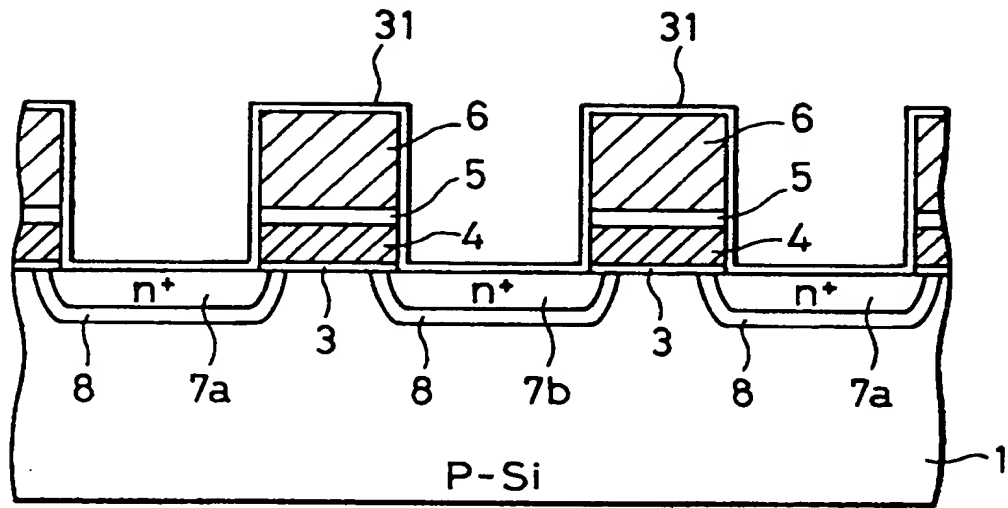


FIG. 5 (a)

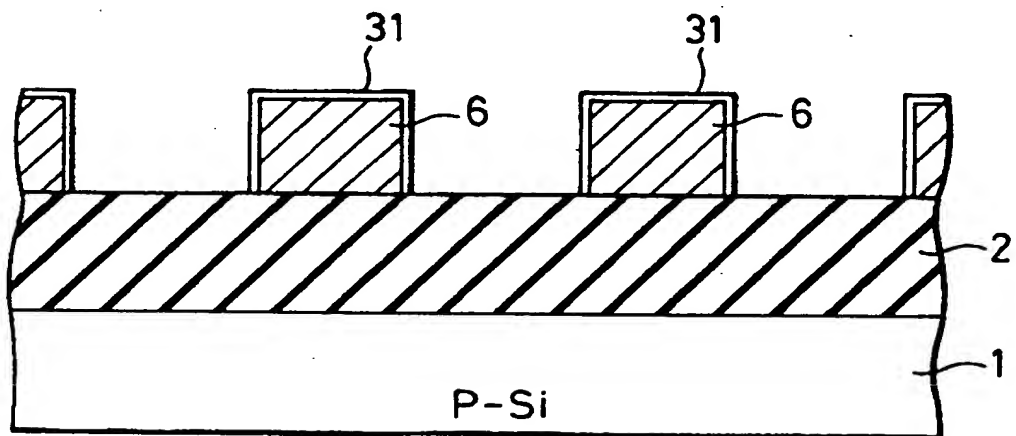


FIG. 5 (b)

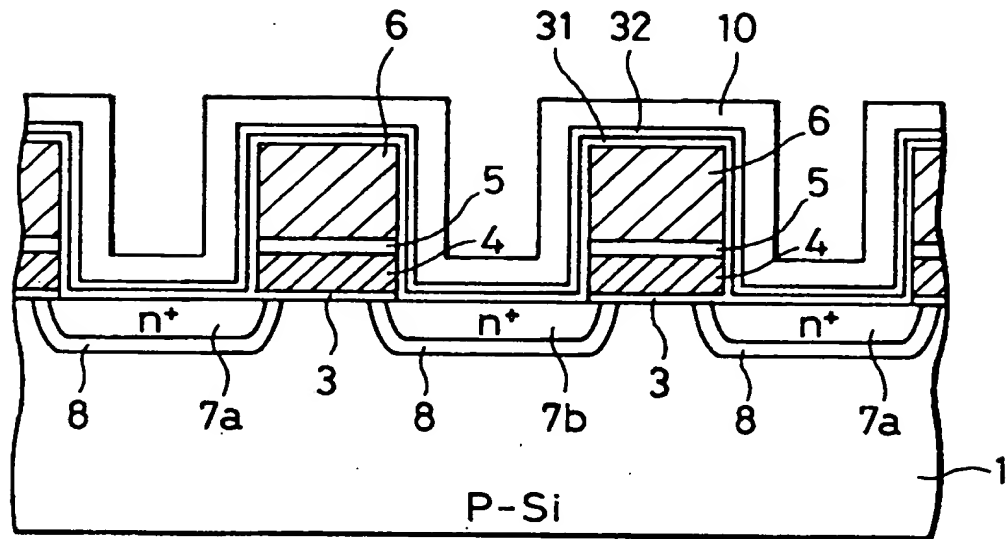


FIG. 6 (a)

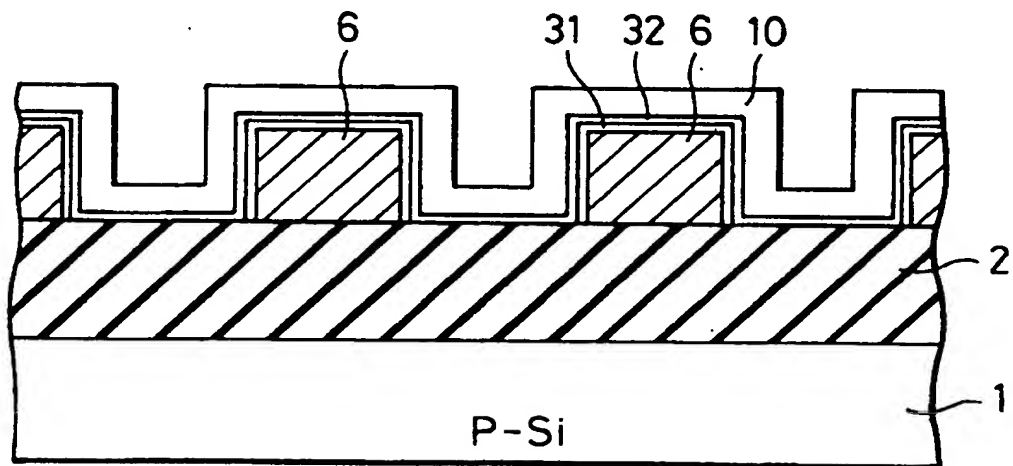


FIG. 6 (b)

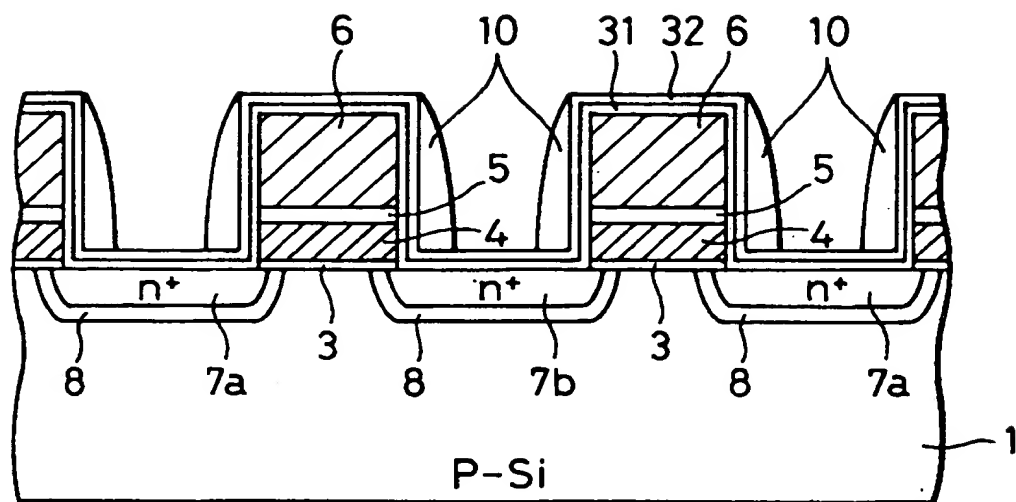


FIG. 7 (a)

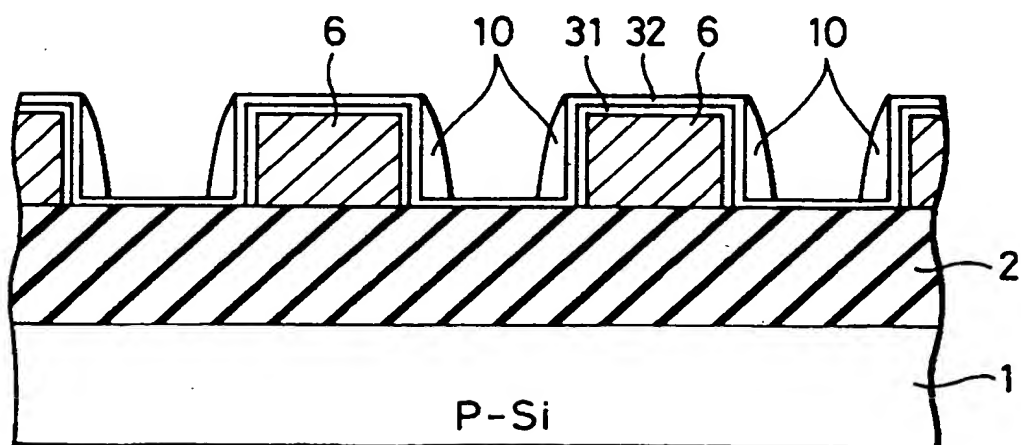


FIG. 7 (b)

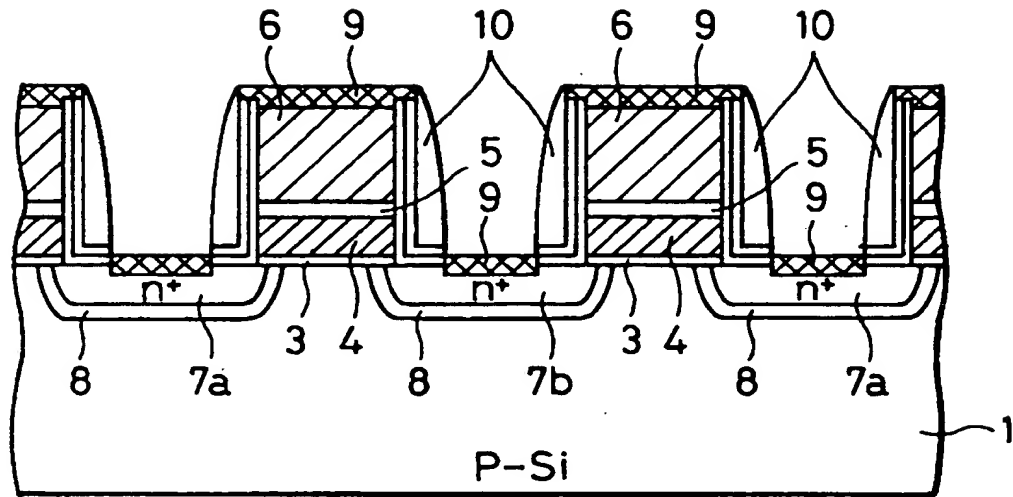


FIG. 8 (a)

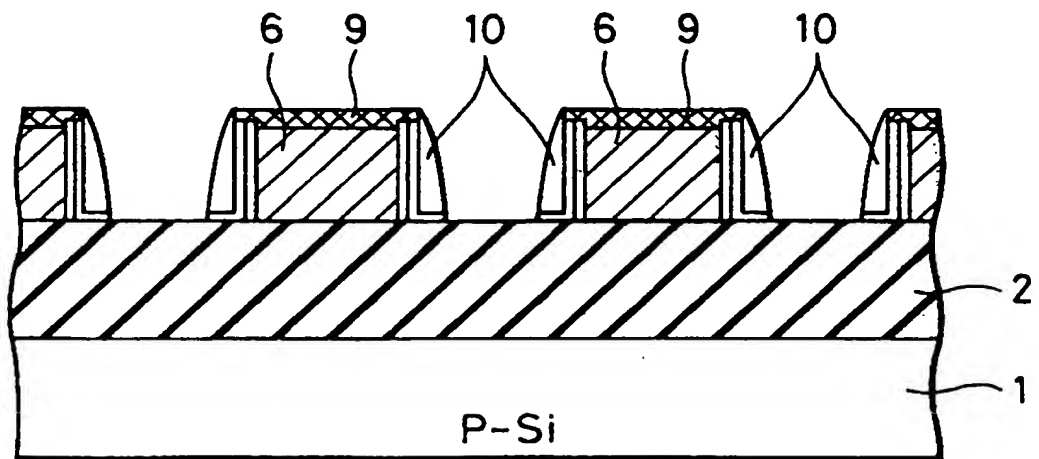


FIG. 8 (b)



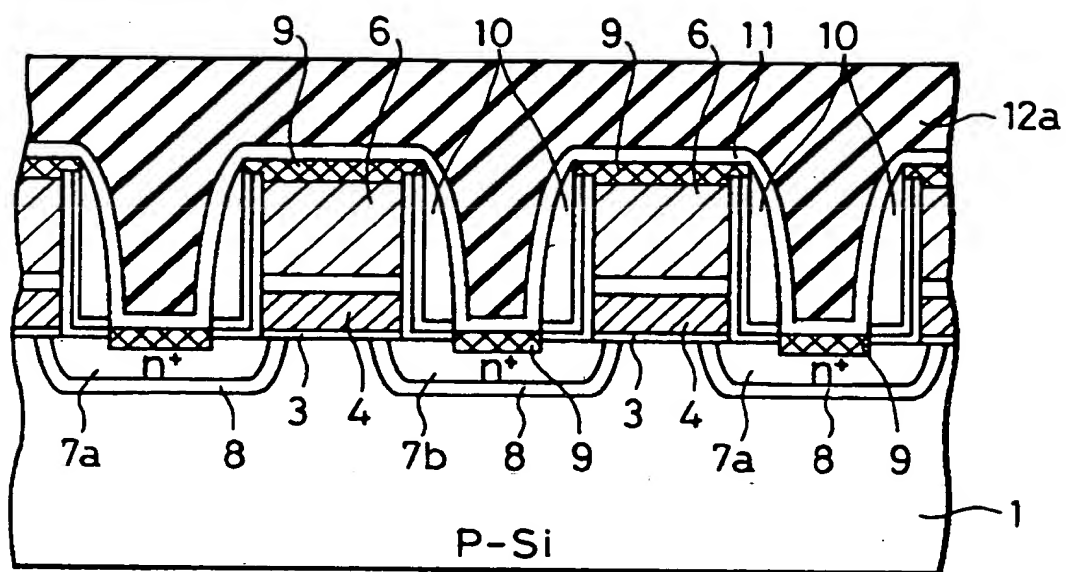


FIG. 9 (a)

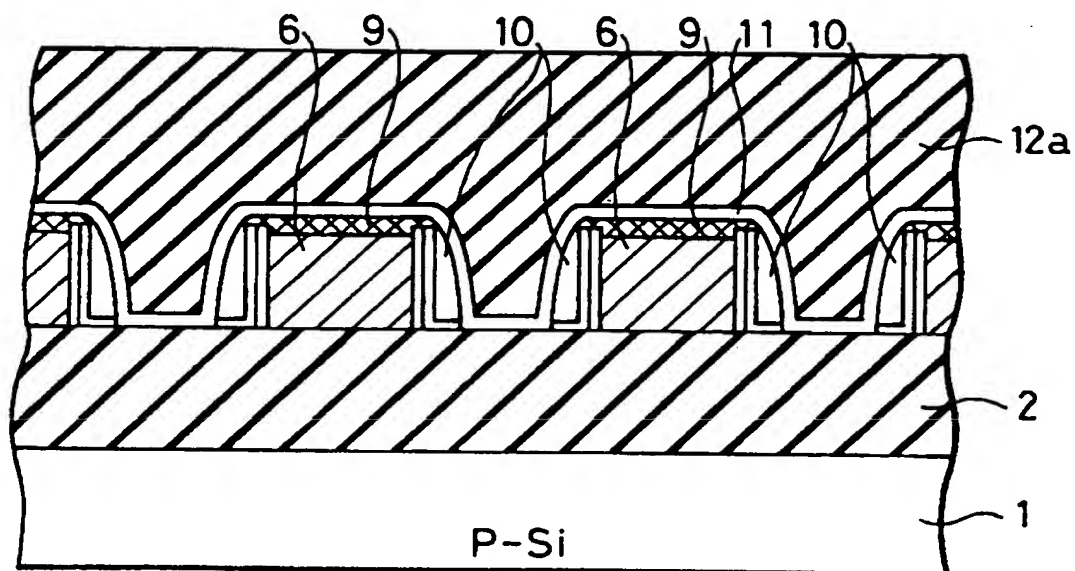
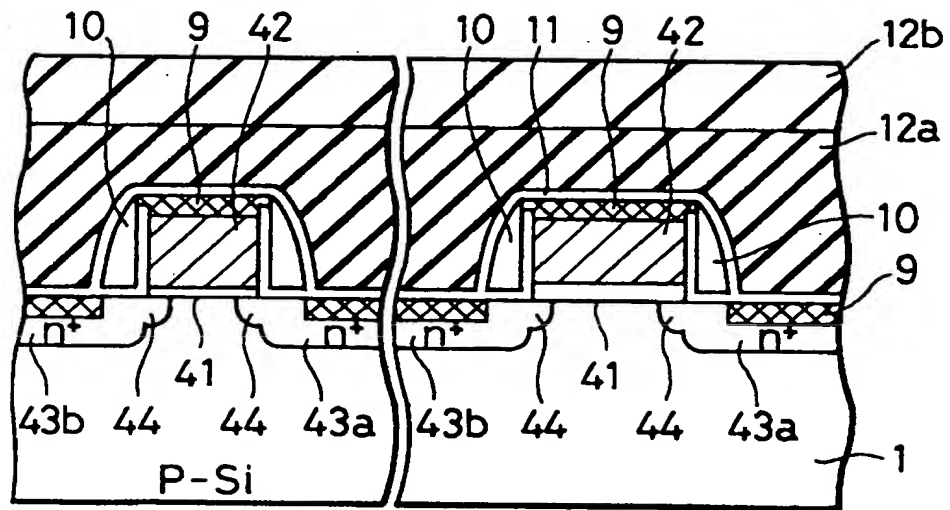


FIG. 9 (b)







[LOW-VOLTAGE MOS]

[HIGH-VOLTAGE MOS]

FIG. 12

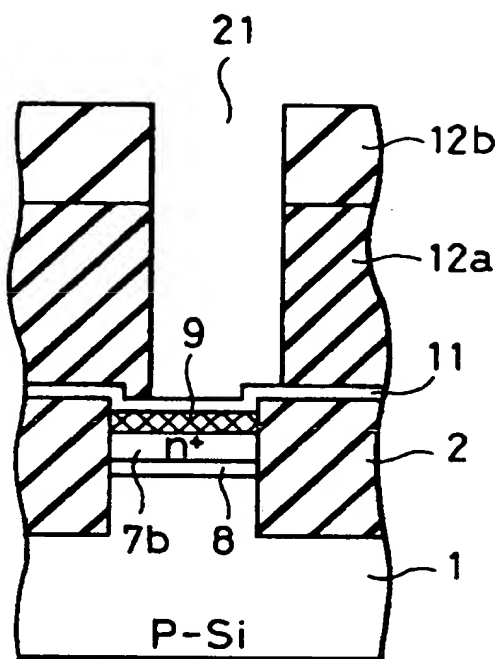


FIG. 13

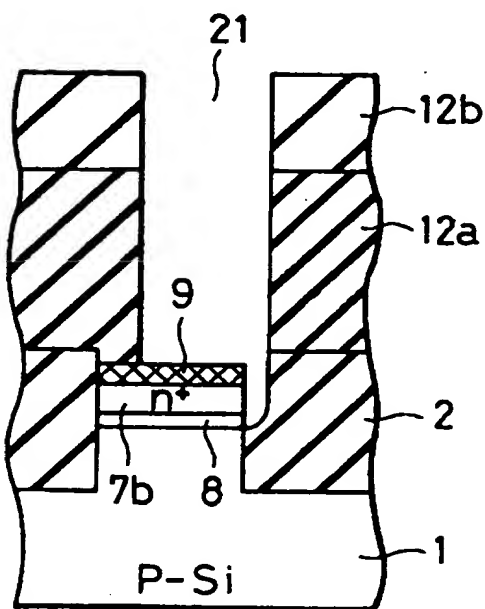


FIG. 14

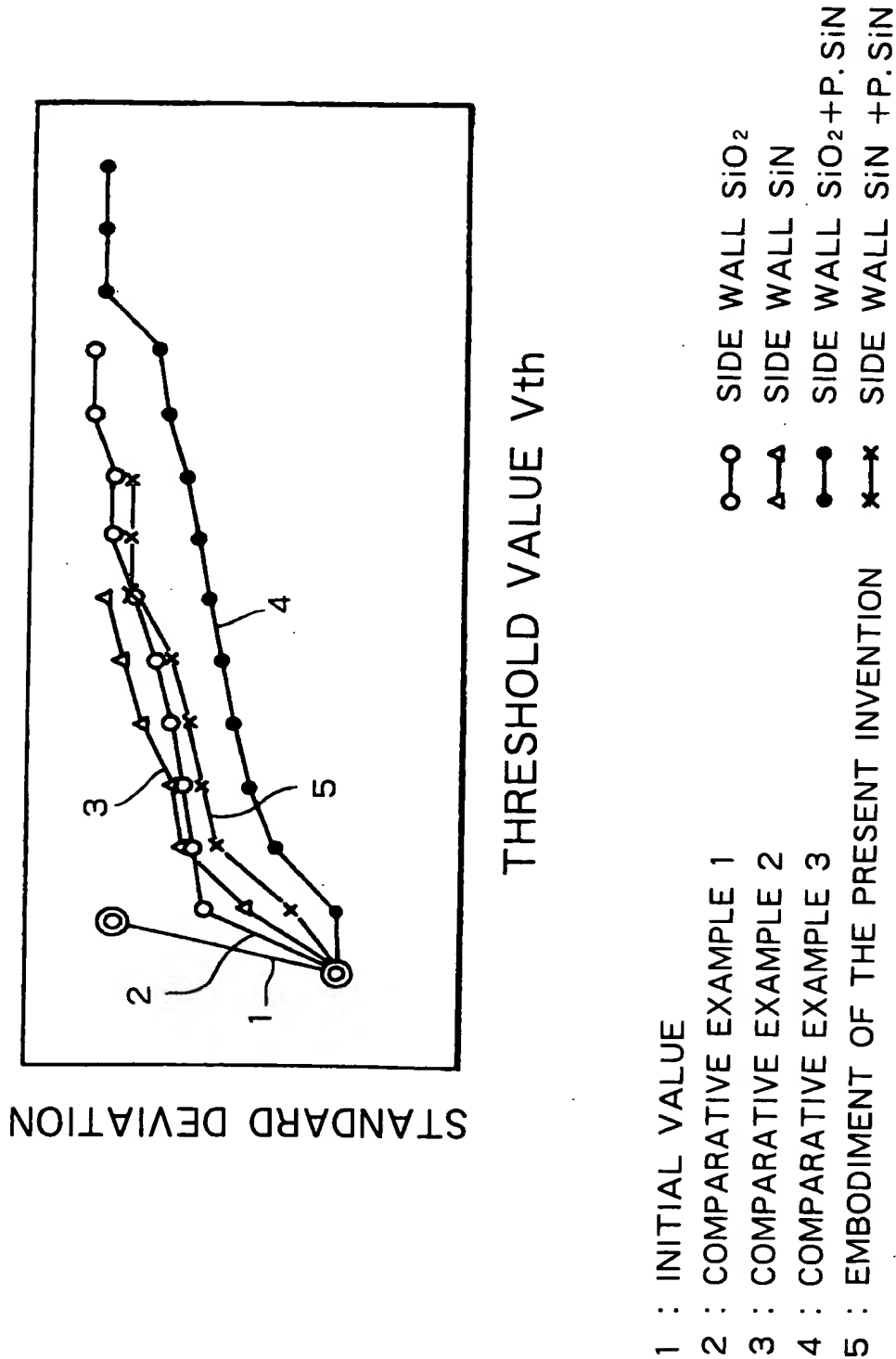


FIG. 15